ABSTRACT

A method of providing a substantially void free layer for one or more flip chip assemblies, or one or more microelectronic components, utilizing a curable encapsulant. Also disclosed is a method of injecting an encapsulant into an assembly and a method of treating a microelectronic component to form a void free layer.

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31. A method of treating an interposer layer for a semiconductor wafer assembly to provide a substantially void free interposer layer, comprising:

disposing a sheet-like, compliant interposer layer between a face surface of a semiconductor wafer and a surface of a substrate such that voids within or at the boundaries of the interposer layer are sealed within the assembly, wherein the substrate is rigid; and

applying pressure to the assembly such that the voids in the interposer layer are substantially eliminated.

32. The method as claimed in claim 31, wherein the pressure applying step is conducted for at time period that is at least one hour.

33. The method as claimed in claim 31, wherein the pressure applying includes gradually increasing the applied the pressure.

34. The method as claimed in claim 31, wherein the applied pressure is between about 10 and 1000 pounds per square inch.

35. A method of creating a substantially void-free interposer layer for a semiconductor wafer having a plurality of microelectronic components, comprising:

injecting an interposer layer into a gap between the wafer and a sheet-like substrate such that voids within or at

the boundaries of the interposer layer are sealed within the gap; and

applying pressure such that the voids in the interposer layer are substantially eliminated.

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36. The method as claimed in claim 35, wherein the pressure applying step is conducted for a time period that is at least one hour.

37. The method as claimed in claim 35, wherein the pressure applying includes gradually increasing the applied pressure.

38. The method as claimed in claim 35, wherein the applied pressure is between about 10 and 1000 pounds per square inch.

39. The method as claimed in claim 35, wherein the microelectronic device is a semiconductor chip or a heat spreader.

40. The method as claimed in claim 35, wherein the microelectronic device is a heat spreader.

41. The method as claimed in claim 35, wherein the microelectronic device is comprised of a support ring encircling a semiconductor chip.